#12

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Attorney's Docket No.: 10417-084001 / F51-134741M/KIK

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Izuo Iida
Serial No. : 09/876,554
Filed : June 7, 2001
Title : METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

Art Unit : Unknown
Examiner : Unknown

Attention: Official Draftsman
Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL OF FORMAL DRAWINGS

Please substitute the enclosed 12 sheets of formal drawings for the corresponding drawings presently in the application.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: June 18, 2001

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June 18, 2001
Date of Deposit

Rose Papetti
Signature

Rose Papetti
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FIG.1

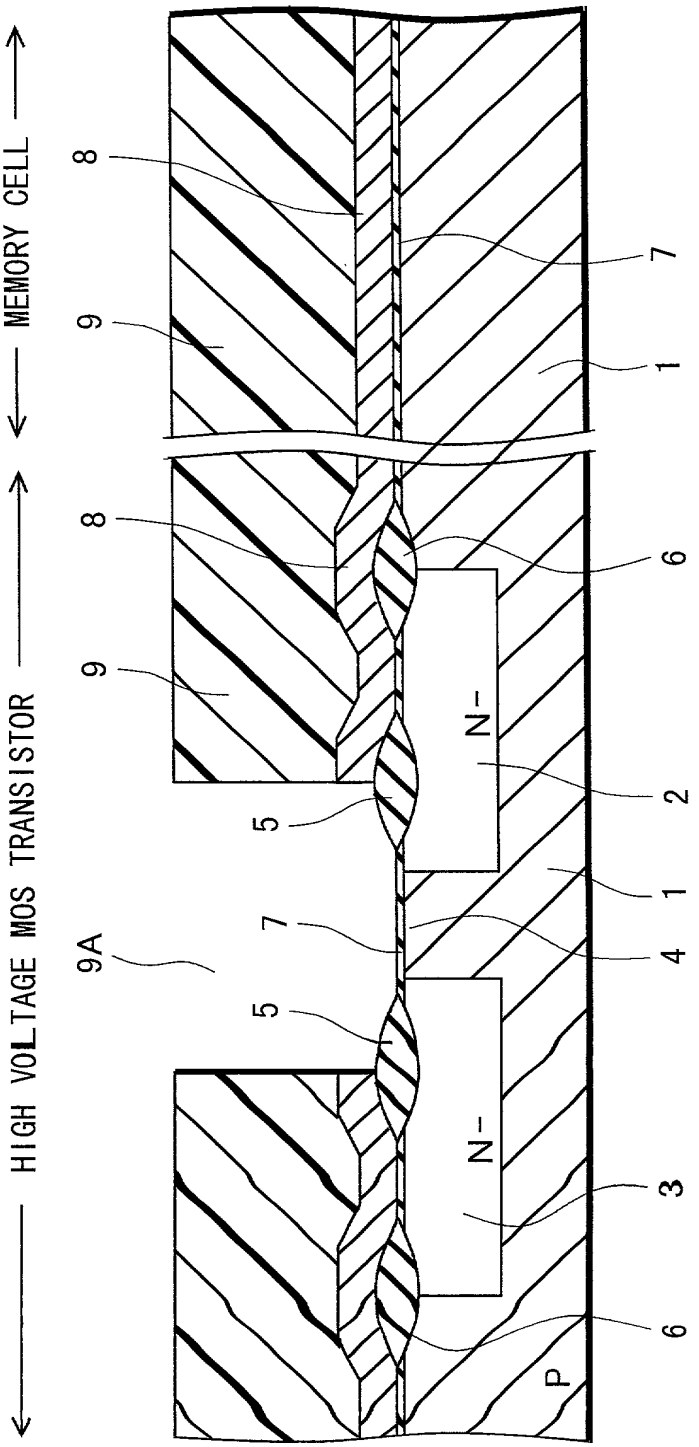
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
8
9
7
1
8
6
9
N-
5
2
1
9A
7
4
5
N-
3
6
P

FIG.2

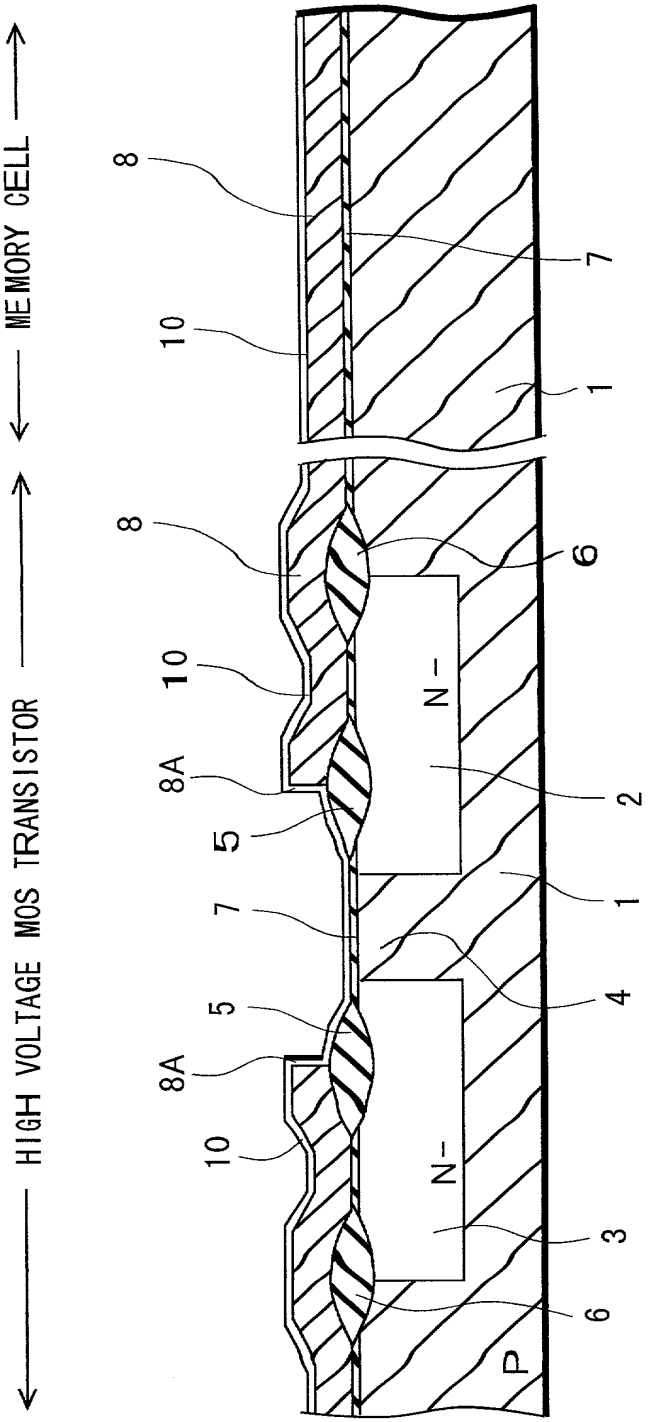
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
8
10
7
1
8
6
10
N-
8A
2
5
1
7
4
5
8A
10
N-
3
6
P

FIG.3

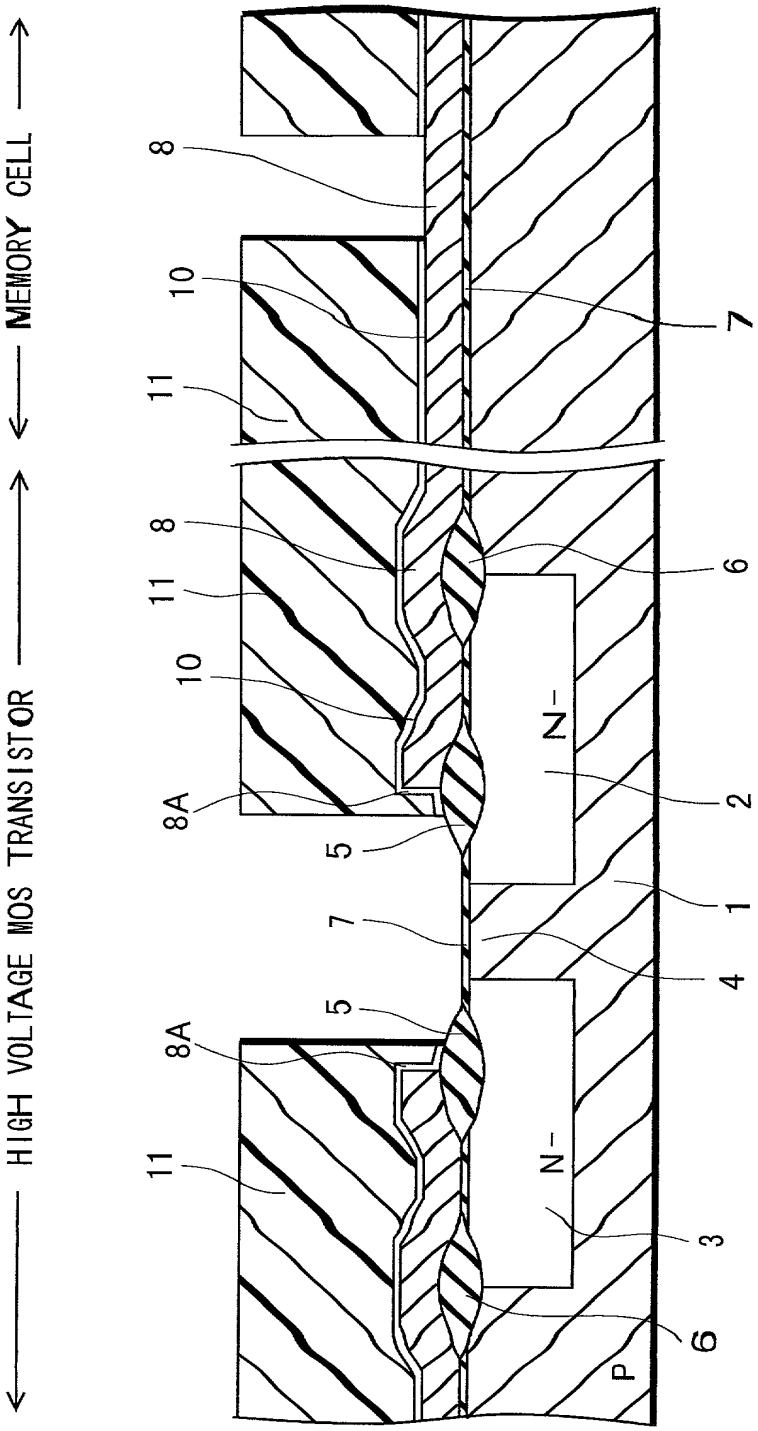
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
8
10
11
7
8
6
11
10
8A
5
N-
2
1
7
4
5
8A
11
N-
3
6
P

FIG.4

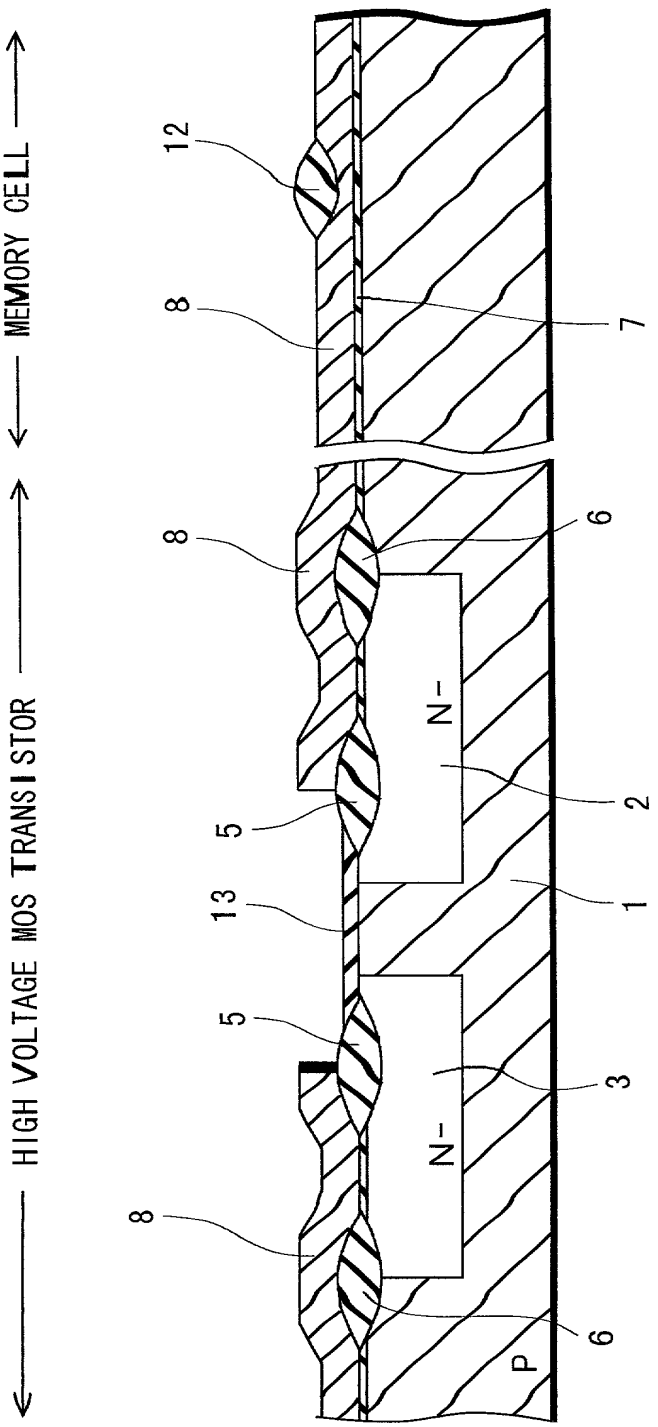
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
12
8
7
8
6
N-
2
5
13
1
5
N-
3
8
6
P

FIG.5

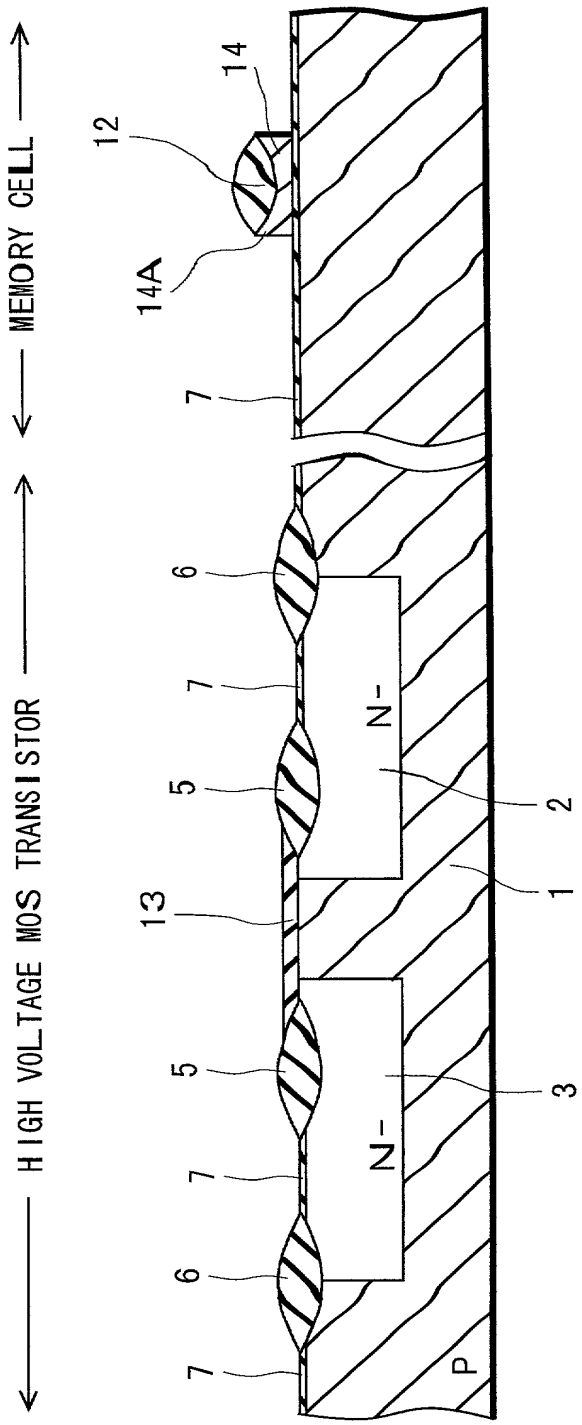
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
12
14
14A
7
6
7
5
13
N-
2
1
5
7
6
7
N-
3
P

FIG.6

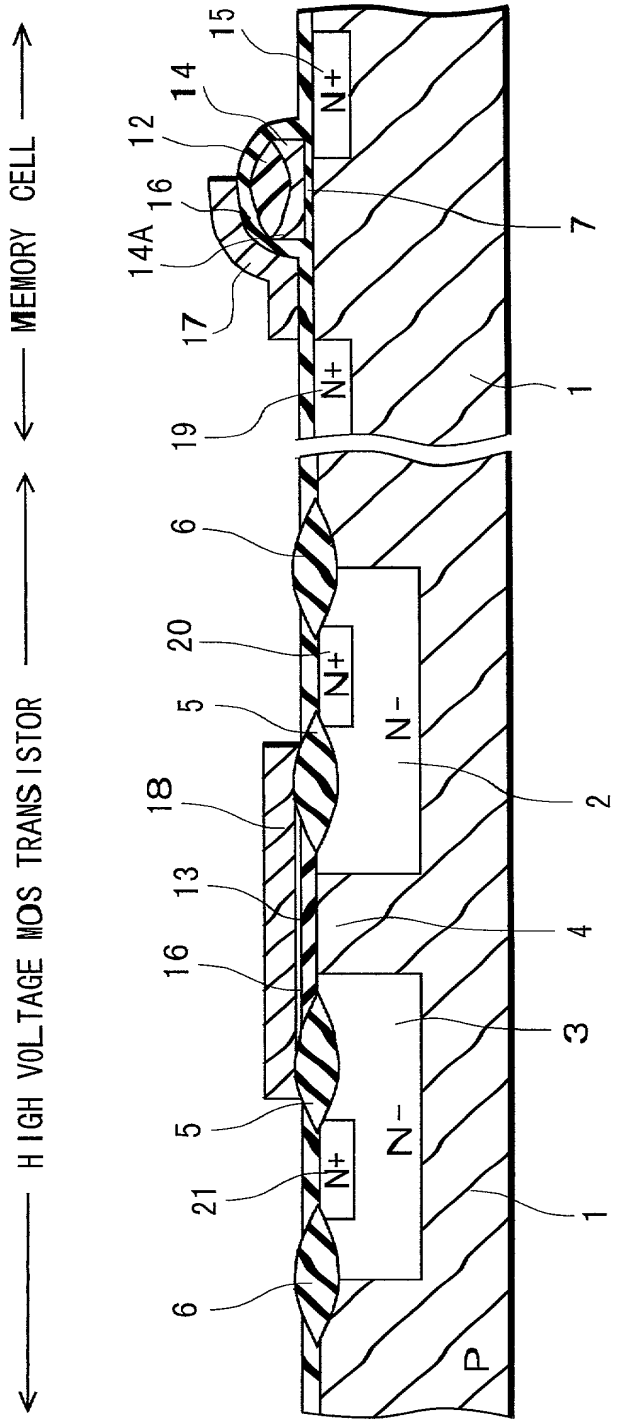
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
N+
N-
P
1
2
3
4
5
6
7
12
13
14
14A
15
16
17
18
19
20
21

FIG.7

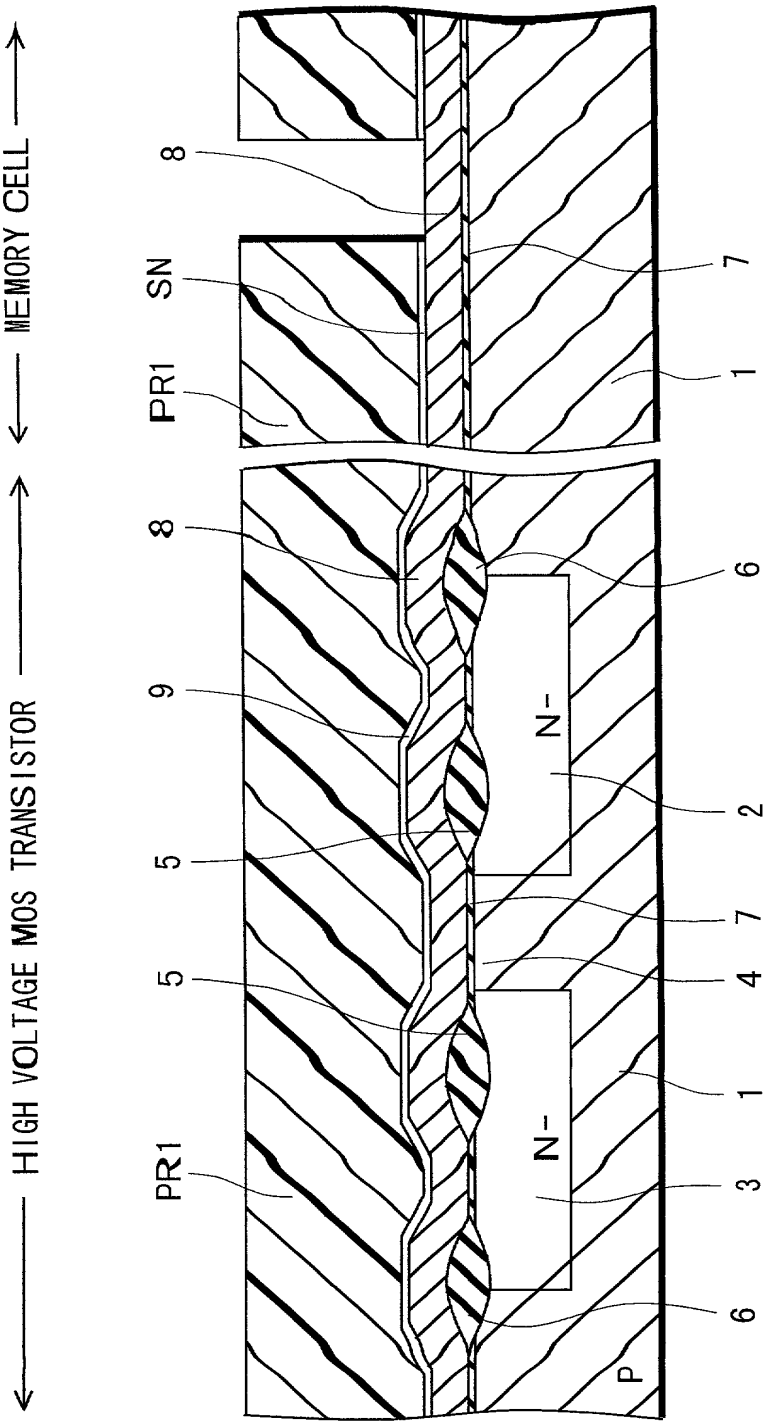
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
PR1
SN
8
7
1
8
6
9
N-
2
5
7
5
4
1
N-
PR1
3
6
P

FIG.8

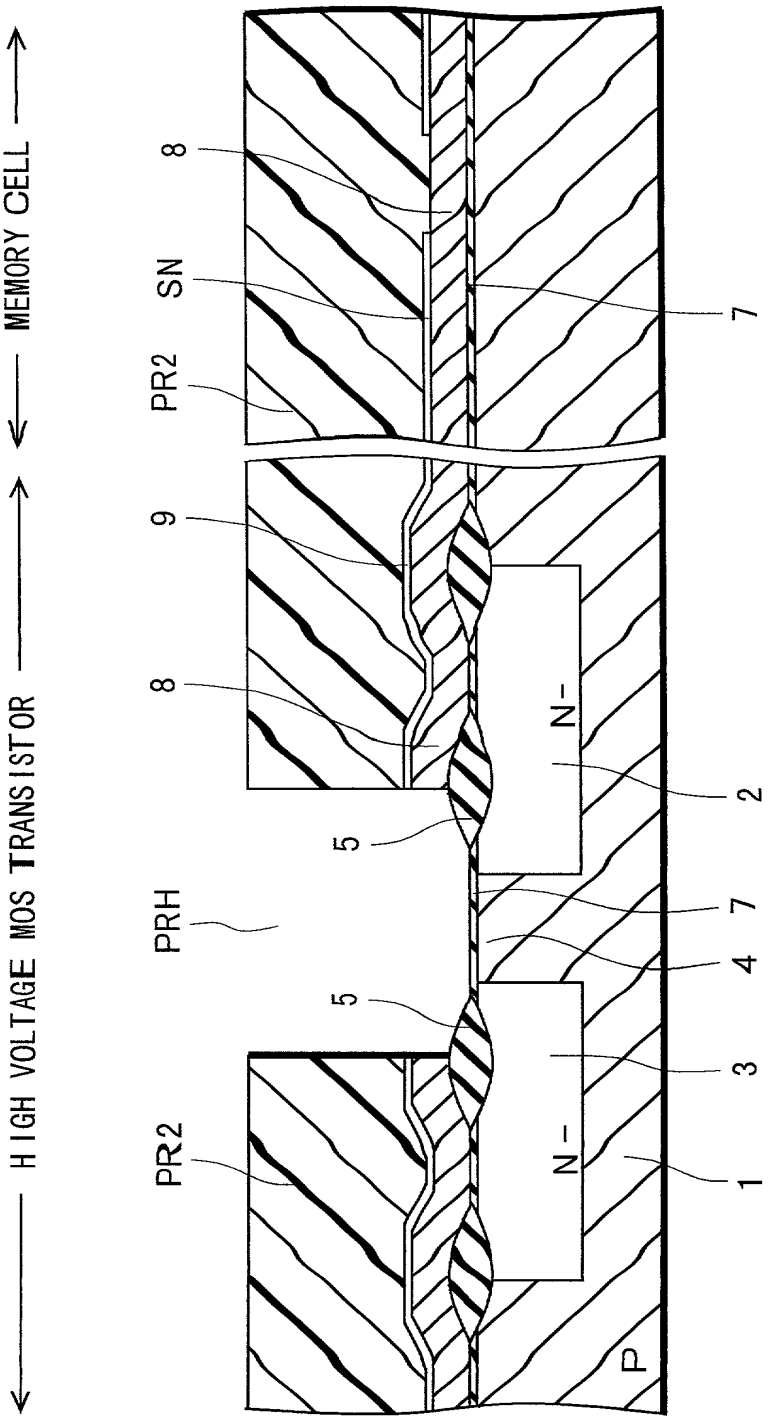
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
PR2
SN
8
7
9
8
N-
2
5
PRH
7
4
5
3
PR2
N-
1
P

FIG.9

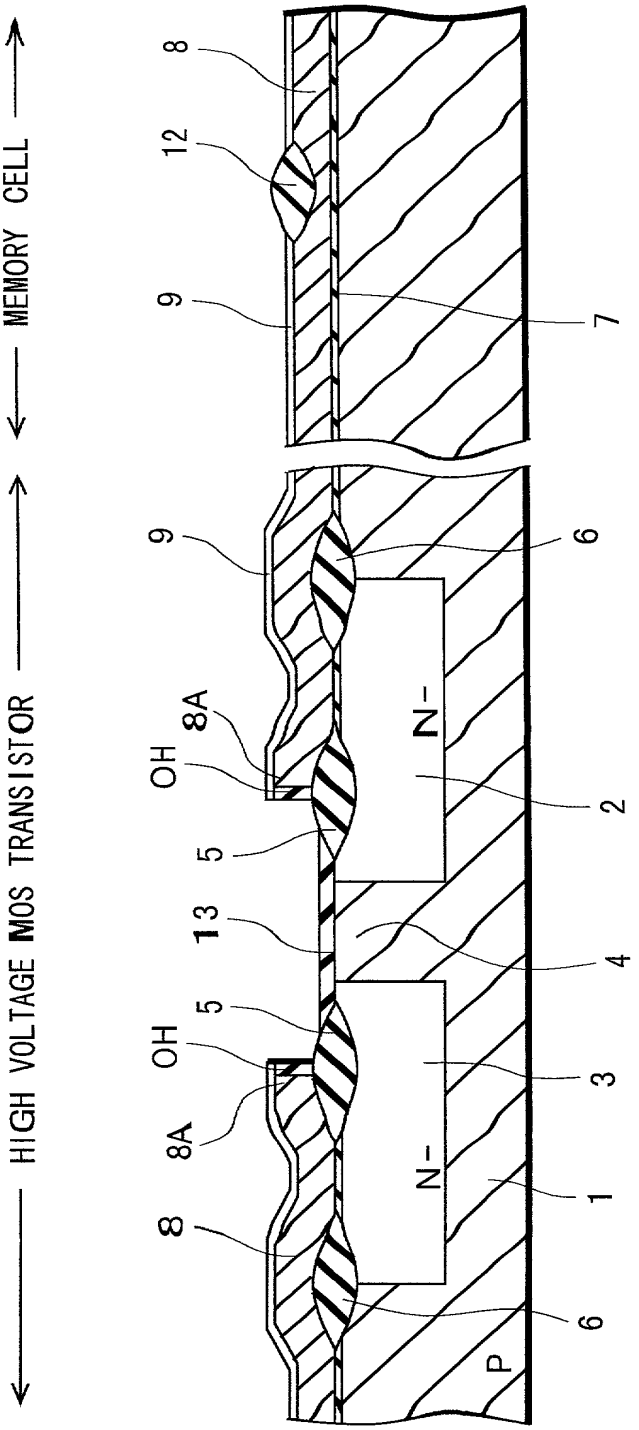
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
8
12
9
7
9
6
OH
8A
N-
2
5
13
4
5
OH
3
8A
N-
1
8
6
P

FIG.10

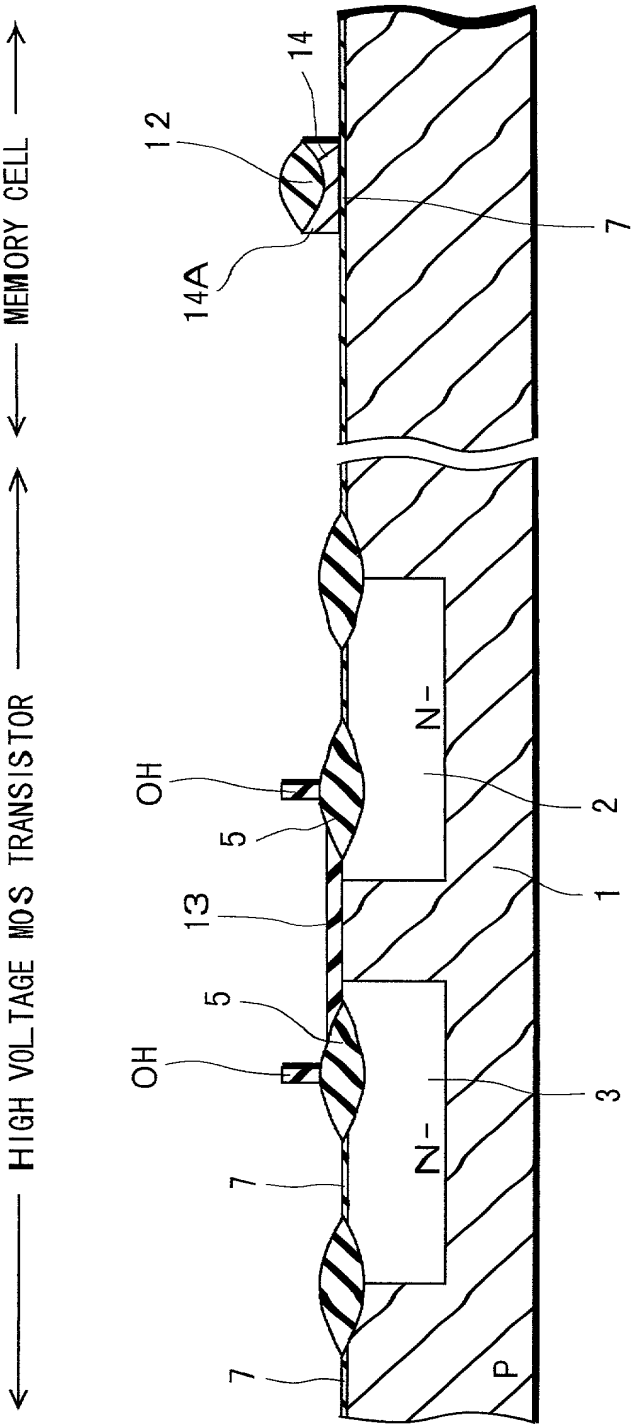
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
12
14
14A
7
OH
5
13
5
OH
7
7
N-
N-
P
2
1
3

FIG.11

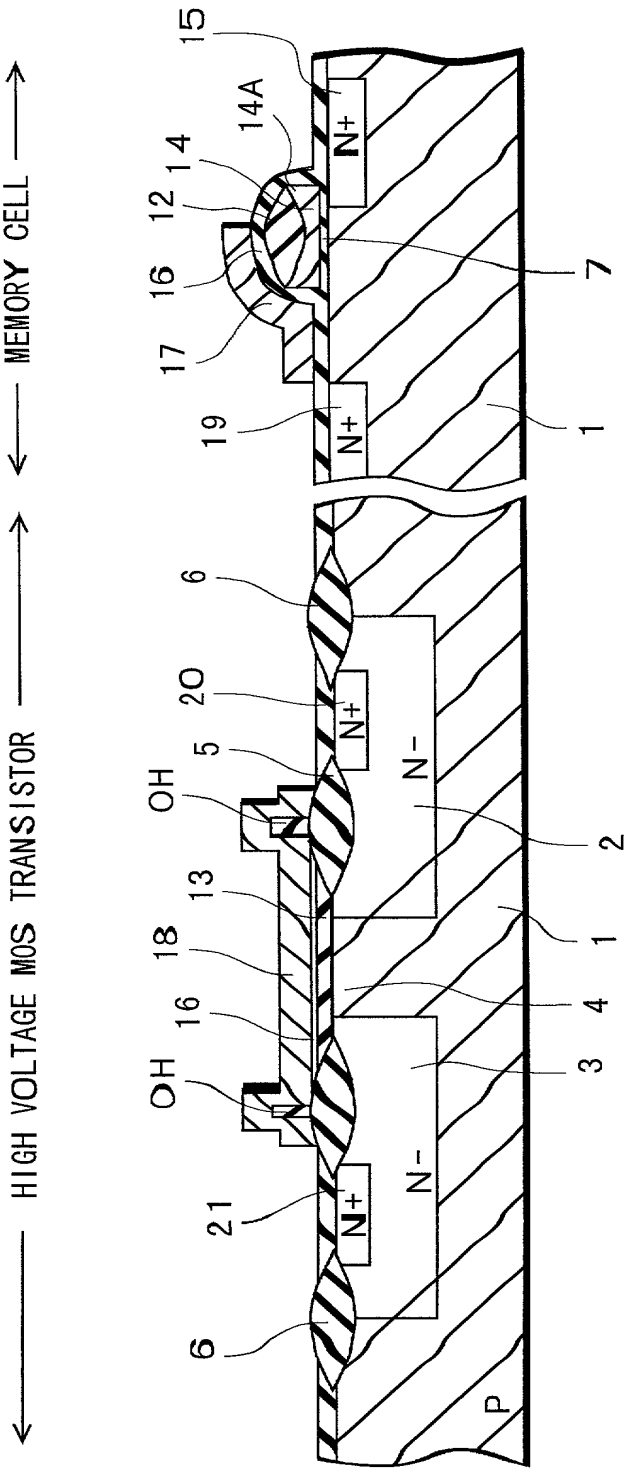
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
N+
N-
P
OH
15
14A
14
12
16
17
19
7
1
6
20
5
2
13
18
4
3
21

FIG.12

PRIOR ART